REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 7-13 and 20-27 are allowable and that claims 15-17 would be allowed if written independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-4, 14, 18, 19, and 28-31 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,991,833 ("Wandler") in view of U.S. Pat. No. 6,684,278 ("Sakugawa"). Claims 5, 6, 32, and 33 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Wandler in view of Sakugawa as applied to claim 1 and claim 28 above and further in view of U.S. Pat. No. 5,845,329 ("Onishi").

As to claims 1 and 28, Applicants note that Wandler discloses the use of memory buffers 508, 510 to buffer data from a central processing unit ("CPU") 25 to a system memory 75, similar to the features shown in Applicants' Figure 1 as prior art. The Examiner reads Wandler as connecting a central processing unit ("CPU") and the north bridge with an internal bus for memory operations. However, Wandler does not suggest the use of an internal bus as claimed. As noted in Page 6, Lines 30-31 and Page 7, Lines 1-7 of the Applicants' disclosure, the bus 76 is "internal" in that the central processing unit 72 and the north bridge use a common protocol. This common bus protocol, for example, may be the native protocol of the central processing unit ("CPU"). As such, the central processing unit 72 and north bridge 74 do not require the drivers 34, 50 or the interfaces 30, 46 of the prior art to perform bus protocol conversions. Eliminating the bus protocol conversions, the drivers 34, 50, and the interfaces 30, 46 allows the north bridge core logic 38 to interface with the system memory at a much higher rate than in prior art systems. (Applicants' Disclosure P. 8, L. 2-6.) For example, the implementation shown in Figure 2 may allow the rate to be 200 to 300 megabytes per second while prior art systems

allow access up to only 100 megabytes per second. (Applicants' Disclosure P. 8, L. 2-6.) As shown, one aspect of the Applicants' invention allows the central processing unit to transfer data more quickly than the Wandler reference permits because, unlike the Applicants' invention, Wandler requires the use of an interface. (*See e.g.* Fig. 4, 502.) Since a central processing unit may perform memory accesses more quickly by utilizing the Applicants' claimed invention, the central processing unit wastes less time waiting for memory accesses, thereby allowing the central processing unit to be more productive. Applicants have accordingly amended their claims to better clarify this inherent aspect of their invention. For this reason alone, the claims are in condition for allowance.

Applicants also respectfully submit that the Wandler reference should not be viewed in light of the Sakugawa reference to obviate Applicants' claims. Sakugawa's invention is aimed at minimizing a microcomputer's power consumption by sacrificing a central processing unit's productivity. (Col. 2, L. 16-21.) Sakugawa uses the access control of a built-in memory 4 to control a central processing unit's power consumption. (Col. 5, L. 57-60.) Sakugawa's memory controller 2 forces a waiting state during a memory access such that a central processing unit is actuated at a low speed, thereby reducing a microcomputer's power consumption. (*Id.*) Sakugawa even goes a step further by suggesting that the memory controller 2 may stop the clock of the central processing unit 1. (Col. 6, L. 21-34.) This is at odds with Applicants' claims.

Applicants' claimed methods, for example, eliminate a need for converting between bus protocols, which eliminates the need for, among other things, some drivers and interfaces between the central processing unit and north bridge. Applicants' claimed methods allow both a central processing unit and memory to operate at their nominal, specified rates without being

slowed down by other components of the system. However, Sakugawa teaches a method for slowing down a processor by having a memory controller intentionally create a bottleneck so that the central processing unit in a microcomputer can conserve power. The Applicants respectfully submit that since their invention is aimed at increasing the efficient, maximum use of a central processing unit, one of ordinary skill in the art would not look to a reference that slows down a central processing unit to solve the problem addressed by Applicants' invention.

In any event, even construing the teachings of the references as suggested, the resulting system, as best understood, would still be a system employing a central processing unit integrated in the north bridge as taught by Wandler with a memory controller that slows down the central processing unit of Wandler as taught by Sakugawa. In contrast, Applicants claim a method for integrating a personal computing system that includes, among other things, "integrating a central processing unit with a north bridge on to a single substrate such that the central processing unit is directly coupled to the north bridge via an internal bus having a bus protocol that is a native bus protocol of the central processing unit" and "providing memory access requests from the central processing unit to the north bridge at a rate of the central processing unit via the internal bus."

Applicants would also like to kindly suggest that portions of the Wandler reference may have been misapprehended. For example, as to claim 2, Wandler is cited as integrating a south bridge onto the same substrate as a central processing unit and a north bridge. (Citing to Fig. 2; Col. 6. Lines 5-7.) However, Figure 2 shows a south bridge 100, north bridge 50, and central processing unit 25 in a computer system 10 having, among other things, a display 62, not a single substrate. (Col. 5, L. 66.) Applicants make similar suggestions regarding the rejections of claim

3 for memory and claim 4 for a graphics controller. As such, these claims are also in condition for allowance.

As to claim 14, Applicants respectfully reassert the relevant remarks made above. For example, the Office Action cites [10] (in Wandler) as the claimed substrate containing both the memory and the north bridge. However, [10] is a computer system 10 with a display 62, not a single substrate. Therefore, Wandler does not teach the claimed structure.

The dependent claims all depend on allowable base claims, add additional novel and nonobvious subject matter, and are believed to be in condition for allowance.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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